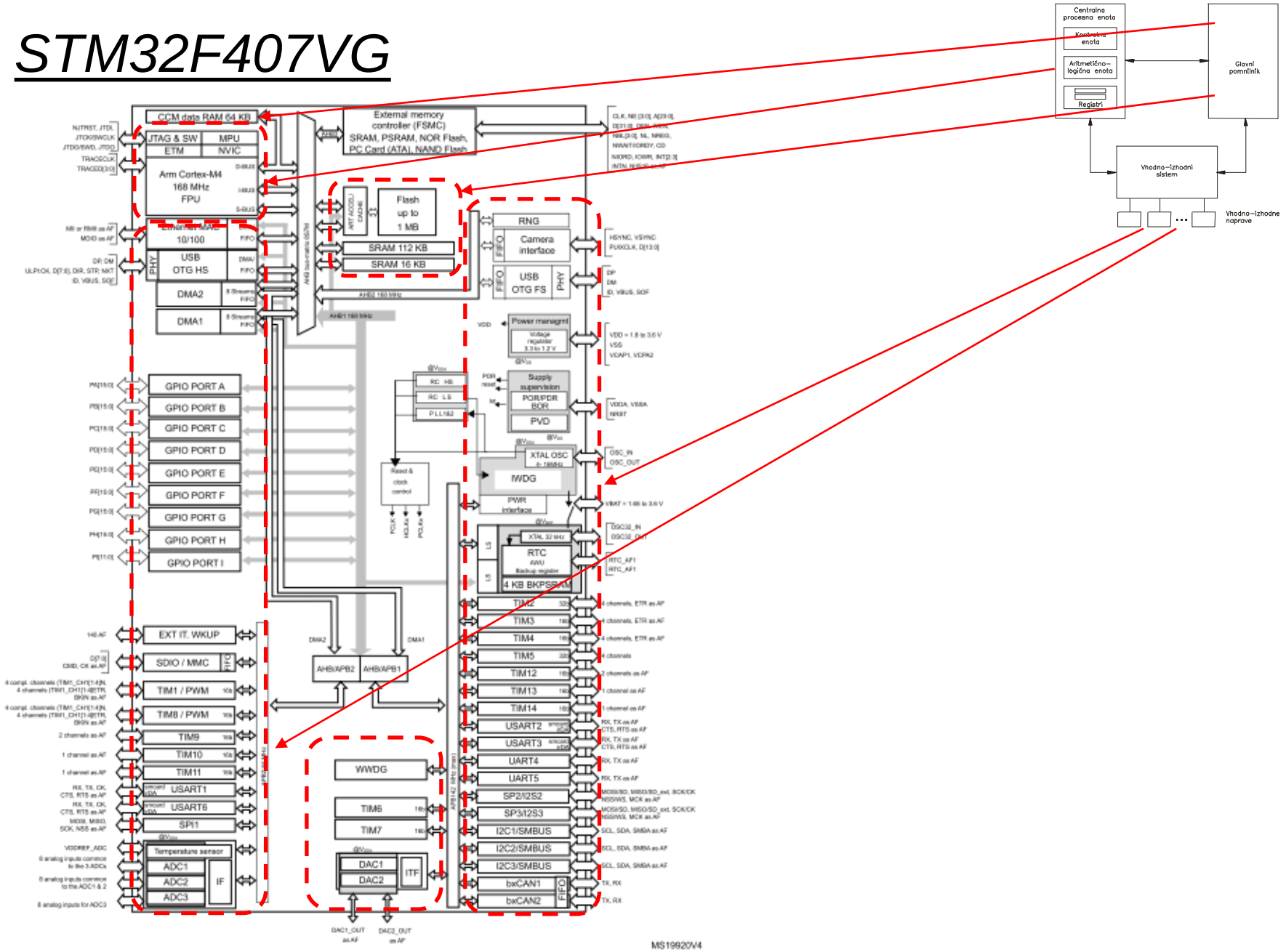
STM32F407 Discovery

Vhodno / izhodne naprave

SysTick Časovnik

STM32F407VG



Delo na STM32F4 razvojnem sistemu

Priključitev :

- **Mini USB** priklop na **krajši stranici**, svetita rdeči **LED** diodi

Poseben začetni projekt za *STM32F4* (e-učilnica) :

- ***dodajanje vsebine (template.s):***

'template.s - STM32CubeIDE

avigate Search Project Run Window Help

template.s

```
54
55 _start:
56     // Enable GPIOD Peripheral Clock (bit 3 in AHB1ENR register)
57     ldr r6, = RCC_AHB1ENR        // Load peripheral clock reg address to r6
58     ldr r5, [r6]                 // Read its content to r5
59     orr r5, #0x00000008           // Set bit 3 to enable GPIOD clock
60     str r5, [r6]                 // Store result in peripheral clock register
61
62     // Make GPIOD Pin12 as output pin (bits 25:24 in MODER register)
63     ldr r6, = GPIOD_MODER        // Load GPIOD MODER register address to r6
64     ldr r5, [r6]                 // Read its content to r5
65     bic r5, #0x3000000           // Clear bits 24, 25 for P12
66     orr r5, #0x01000000          // Write 01 to bits 24, 25 for P12
67     str r5, [r6]                 // Store result in GPIOD MODER register
68
69     // Set GPIOD Pin12 to 1 (bit 12 in ODR register)
70     ldr r6, = GPIOD_ODR          // Load GPIOD output data register
71     ldr r5, [r6]                 // Read its content to r5
72     orr r5, #0x1000               // write 1 to pin 12
73     str r5, [r6]                 // Store result in GPIOD output data register
74
75     // Set GPIOD Pin12 to 0 (bit 12 in ODR register)
76     ldr r6, = GPIOD_ODR          // Load GPIOD output data register
77     ldr r5, [r6]                 // Read its content to r5
78     bic r5, #0x1000              // write 0 to pin 12
79     str r5, [r6]                 // Store result in GPIOD output data register
80
81 loop:
82     nop                          // No operation. Do nothing.
83     b loop                       // Jump to loop
84
```

STM32 CubeIDE, STM32F4 (izbrana dokumentacij

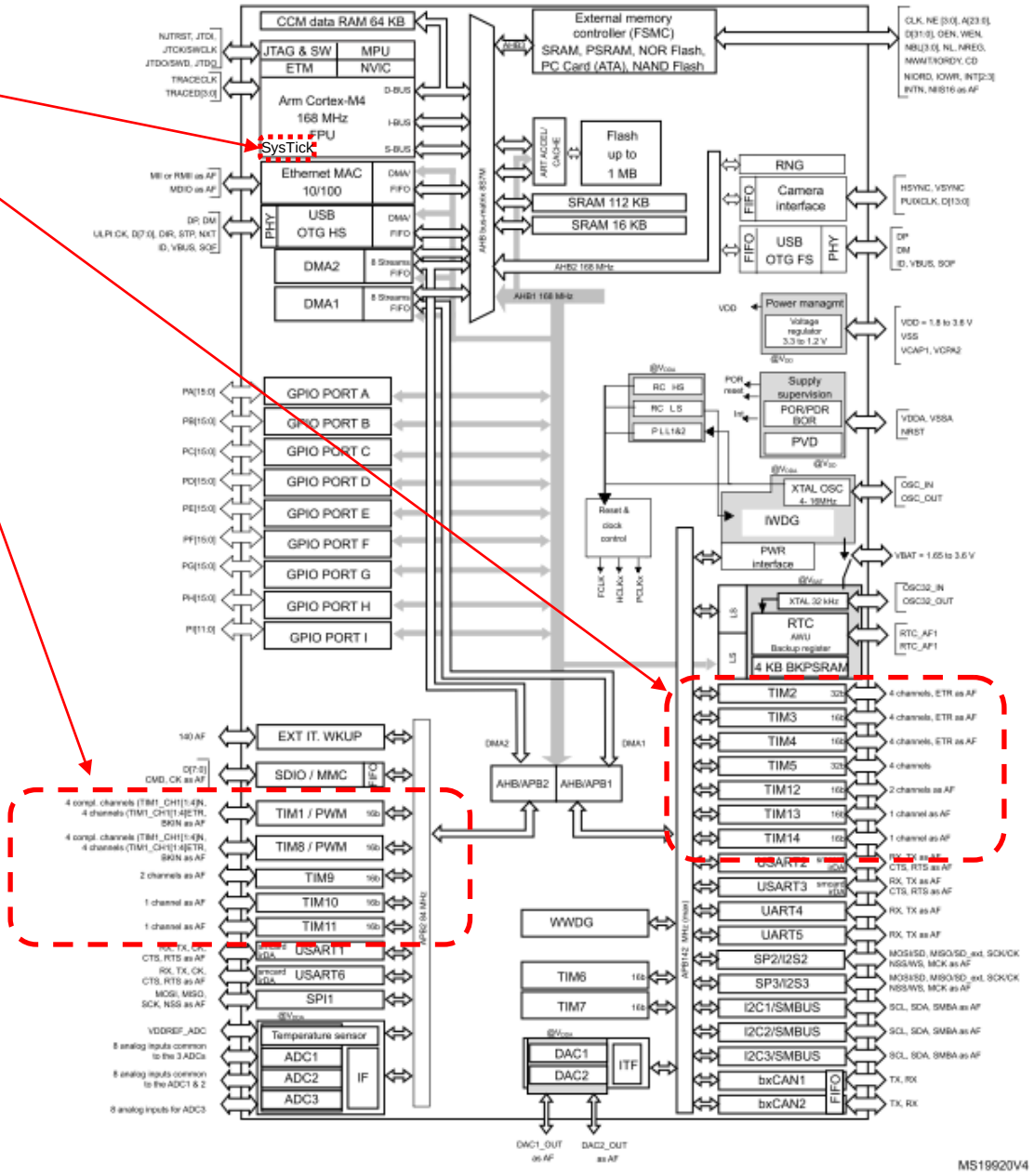
--------- Razvojni sistem ----------

- STM32 CubeIDE
- ORLab-STM32 - GitHub repozitorij
- User Manual Discovery kit stm32f407vg Uploaded 8/11/21, 12.58
- DataSheet_stm32f407vg Uploaded 8/11/21, 12.56
- Reference Manual rm0090-stm32f407417 Uploaded 8/11/21, 12.57
- Programming_Manual_pm0214-stm32-cortexm4-mcus-and-mpu
- Arm Cortex-M4 Processor Datasheet Short Uploaded 29/10/21, 15.00

--------- Cortex-M arhitektura, zbirnik ----------

- ARM Cortex-M for Beginners ARM 2017 Uploaded 29/10/21, 14.50

Časovniki


CCM data RAM 64 KB
JTAG & SW
ETM
MPU
NVIC
Arm Cortex-M4
168 MHz
FPU
SysTick
Ethernet MAC
10/100
USB
OTG HS
DMA2
DMA1
External memory
controller (FSMC)
SRAM, PSRAM, NOR Flash,
PC Card (ATA), NAND Flash
Flash
up to
1 MB
SRAM 112 KB
SRAM 16 KB
RNG
Camera
interface
USB
OTG FS
Power managmt
Supply
supervision
POR/PDR
BOR
PVD
XTAL OSC
4- 26MHz
IWDG
PWR
interface
XTAL 32 kHz
RTC
AWU
Backup register
4 KB BKPSRAM
GPIO PORT A
GPIO PORT B
GPIO PORT C
GPIO PORT D
GPIO PORT E
GPIO PORT F
GPIO PORT G
GPIO PORT H
GPIO PORT I
EXT IT. WKUP
SDIO / MMC
TIM1 / PWM
TIM8 / PWM
TIM9
TIM10
TIM11
USART1
USART6
SPI1
Temperature sensor
ADC1
ADC2
ADC3
IF
AHB/APB2
AHB/APB1
WWDG
TIM6
TIM7
DAC1
DAC2
ITF
TIM2
TIM3
TIM4
TIM5
TIM12
TIM13
TIM14
USART2
USART3
UART4
UART5
SP2/I2S2
SP3/I2S3
I2C1/SMBUS
I2C2/SMBUS
I2C3/SMBUS
bxCAN1
bxCAN2
MS19920V4

Vira: Reference & Programming manuals

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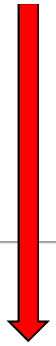
PM0214
Programming manual

STM32 Cortex®-M4 MCUs and MPUs programming manual



Core peripherals PM0214

4.5 SysTick timer (STK)

Table 54. System timer registers summary

Address	Name	Type	Required privilege	Reset value	Description
0xE000E010	STK_CTRL	RW	Privileged	0x00000000	*SysTick control and status register (STK_CTRL) on page 247*
0xE000E014	STK_LOAD	RW	Privileged	Unknown	*SysTick reload value register (STK_LOAD) on page 248*
0xE000E018	STK_VAL	RW	Privileged	Unknown	*SysTick current value register (STK_VAL) on page 249*
0xE000E01C	STK_CALIB	RO	Privileged	0xC0000000	*SysTick calibration value register (STK_CALIB) on page 250*

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RM0090
Reference manual

STM32F405/415, STM32F407/417, STM32F427/437 and STM32F429/439 advanced Arm®-based 32-bit MCUs

17 Advanced-control timers (TIM1 and TIM8)

18 General-purpose timers (TIM2 to TIM5)

19 General-purpose timers (TIM9 to TIM14)

20 Basic timers (TIM6 and TIM7)

21 Independent watchdog (IWDG)

22 Window watchdog (WWDG)

SysTick časovnik – stanje , nastavitve

4.5.6 SysTick register map

The table provided shows the SysTick register map and reset values. The base address of the SysTick register block is 0xE000 E010.

Table 55. SysTick register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	STK_CTRL	Reserved															COUNTFLAG	Reserved													CLKSOURCE	TICKINT	ENABLE
	Reset Value																0														1	0	0
0x04	STK_LOAD	Reserved															RELOAD[23:0]																
	Reset Value																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	STK_VAL	Reserved															CURRENT[23:0]																
	Reset Value																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	STK_CALIB	Reserved															TENMS[23:0]																
	Reset Value																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Osnovni registri za delovanje SysTick časovnika:

STK_CTRL : vklop časovnika

CLKSOURCE=1, ENABLE=1

COUNTERFLAG=1, ko prešteje do 0 (postavi na STK_LOAD in nadaljuje)

STK_LOAD : zač. vrednost štetja (šteje proti 0)

STK_LOAD = število period

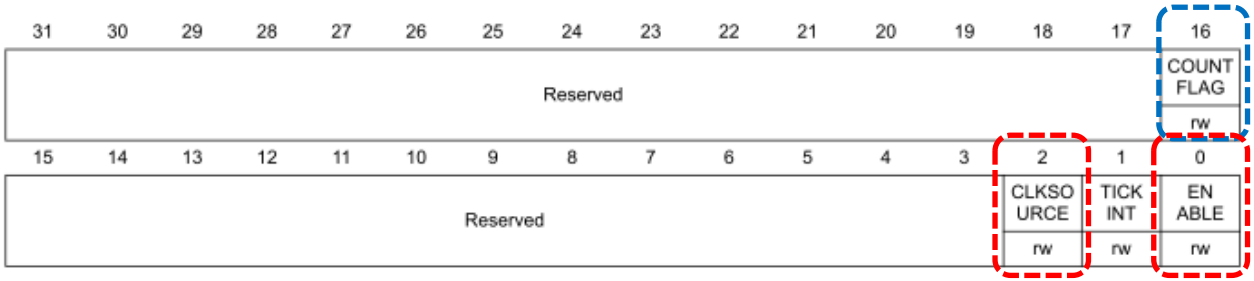
STK_VAL : trenutna vrednost števca

STK_VAL = nekje med STK_LOAD in 0

SysTick časovnik *(Registri za nastavitve delovanja)*

4.5.1 SysTick control and status register (STK_CTRL)

Address offset: 0x00



Bit 16 COUNTFLAG:
Returns 1 if timer counted to 0 since last time this was read.

Bits 15:3 Reserved, must be kept cleared.

Bit 2 **CLKSOURCE:** Clock source selection
Selects the clock source.
0: AHB/8
1: Processor clock (AHB)

Bit 1 **TICKINT**: SysTick exception request enable
0: Counting down to zero does not assert the SysTick exception request
1: Counting down to zero to asserts the SysTick exception request.
Note: Software can use COUNTFLAG to determine if SysTick has ever counted to zero.

Bit 0 **ENABLE**: Counter enable
Enables the counter. When ENABLE is set to 1, the counter loads the RELOAD value from the LOAD register and then counts down. On reaching 0, it sets the COUNTFLAG to 1 and optionally asserts the SysTick depending on the value of TICKINT. It then loads the RELOAD value again, and begins counting.
0: Counter disabled
1: Counter enabled

SysTick časovnik *(Registri za nastavitve delovanja)*

4.5.2 SysTick reload value register (STK_LOAD)

Address offset: 0x04

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								RELOAD[23:16]							
								rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RELOAD[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:24 Reserved, must be kept cleared.

Bits 23:0 **RELOAD:** RELOAD value

The LOAD register specifies the start value to load into the STK_VAL register when the counter is enabled and when it reaches 0.

Calculating the RELOAD value

The RELOAD value can be any value in the range 0x00000001-0x00FFFFFF. A start value of 0 is possible, but has no effect because the SysTick exception request and COUNTFLAG are activated when counting from 1 to 0.

The RELOAD value is calculated according to its use:

- To generate a multi-shot timer with a period of N processor clock cycles, use a RELOAD value of N-1. For example, if the SysTick interrupt is required every 100 clock pulses, set RELOAD to 99.
- To deliver a single SysTick interrupt after a delay of N processor clock cycles, use a RELOAD of value N. For example, if a SysTick interrupt is required after 100 clock pulses, set RELOAD to 99.

SysTick časovnik *(Registri za nastavitve delovanja)*

4.5.3 SysTick current value register (STK_VAL)

Address offset: 0x08

Reset value: 0x0000 0000

Required privilege: Privileged

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								CURRENT[23:16]							
								rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CURRENT[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:24 Reserved, must be kept cleared.

Bits 23:0 **CURRENT:** Current counter value

The VAL register contains the current value of the SysTick counter.

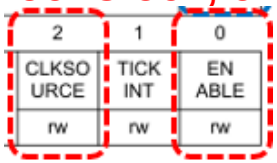
Reads return the current value of the SysTick counter.

A write of any value clears the field to 0, and also clears the COUNTFLAG bit in the STK_CTRL register to 0.

SysTick Časovnik – krmiljenje

Potrebni koraki za krmiljenje časovnika SysTick:

1. **STK_LOAD (Reload Value Register): Value** SYSTICK_RELOAD_1MS
2. **STK_VAL (Current Value Register): 0, reset to zero**
3. **STK_CTRL (Control/Status Register): 0b101 : Proc. Clock, enable**
   -> Start SysTick



4. **Delovanje:**
   Čakanje na pojavitev COUNT_FLAG=1 (b_{16}) v STK_CTRL

Naslovi registrov:

```
// RCC   base address is 0x40023800
//   AHB1ENR register offset is 0x30
.equ     RCC_AHB1ENR,   0x40023830 // RCC AHB1 peripheral clock reg (page 180)

// SysTick Timer definitions
.equ    SCS_BASE, 0xe000e010
.equ    STK_STRL,        0x00 // Control/Status register
.equ    STK_LOAD,        0x04 // Value to countdown from
.equ    STK_VAL,         0x08 // Current value
```

CubeIDE – Registers okno

Name	Value
General Registers	
r0	0x0
r1	0x0
r2	0x0
r3	0x0
r4	0x0
r5	0x1000
r6	0x40020c14
r7	0x0
r8	0x0
r9	0x0
r10	0x0
r11	0x0
r12	0x0
sp	0x20020000
lr	0xffffffff
pc	0x800002a
xpsr	0x41000000

CubeIDE – SFR okno