RA –Additional auditory exercises - Transfers

1. We are transferring 32B (bytes) large blocks between L1 and L2 cache over the 256-bit bus (256 wires). One transfer takes 8 (eight) clock cycles.

- How many clock cycles are required to transfer one block?

  256 bits equal to 32B (bytes), therefore 8 clock cycles

- What is the bandwidth for this bus if the clock frequency equals to 2,5 GHz?

  B = (f / clock_cycles_for_one_transfer) * bus_width =

  = 2,5 * 10**9 [1/s] / 8 * 32 [B] = 10 [GB/s]

2. The processor and the PC12800 DDR3 memory module are connected with a 64-bit data bus. The frequency of the clock signal on the bus is 800 MHz.

- What is the maximal number of transfers per second if transfer executes on a rising and falling edge of clock signal (twice in one cycle).

Transfers per second [T/s] = f * transfers_per_clock_cycle =

= 800 * 106 [1/s] * 2 = <u>1600 [MT/s]</u>**

- What is the bandwidth of this bus? (1M =10^6)?

64b = 8B
B = 1600 * 106 [T/s] * 8 [B/T] = 12800 [MB/s] = <u>12,8 [GB/s]</u> (--> name PC12800)**
or as in previous assignment :
B = 800 * 106 [1/s] / 0.5 * 8 [B] = <u>12800 [MB/s]</u> = <u>12,8 [GB/s]</u>**

3. We are comparing two processors. First operates with a clock frequency of 1GHz, and the other with a clock frequency of 2,6 GHz. A conditional branch takes 3 clock cycles on both processors. How long does it take to execute a conditional branch on both machines?

1. **f=1GHz -> t_{cpe} = 1 ns -> Tukaza = 3 * t_{cpe} = <u>3 ns</u>**
2. **f=2,6GHz -> t_{cpe} = 1/f = 0,38 ns -> Tukaza = 3 * t_{cpe} = <u>1,14 ns</u>**